STIC Search Report
EIC 2800

STIC Database Tracking Number: 129230

TO: Monica Lewis **Location: JEF-5A30** **August 12, 2004** **Case Serial No. : 10/013,103**	**From: Jeff Harrison** **Location: STIC-EIC2800** **JEF-4B68** **Phone: 22511** **Email: harrison, jeff**

Search Notes

Monica,

Attached are the closest of the edited search results from Chemical Abstracts and full-text EP/WO/PCT databases.

Based on this, if you have questions or comments, or if would like refocused searching, please let me know.

Thanks,
Jeff Harrison
Team Leader, STIC-EIC2800
JEF-4B68, 571-272-2511

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact*:**

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

```
    CAS/STN FILE 'HCAPLUS, WPIX' ENTERED AT 14:33:48 ON 12 AUG 2004
L1            2     S       US6352940/PN
L2                  SEL PLU=ON  L1 1- PRN :        1 TERM
L3            3     S       L2
L4                  SEL PLU=ON  L3 1- IC RN :       12 TERMS
L5      1142392     S       L4
L6            3     S       L5 AND L3
                    E PASSIVATION/CT
L7         3118     S       "SURFACE TREATMENT"/CT
L8        43461     S       PASSIVATION/CT OR "PASSIVATION KINETICS"/CT OR PASSIVITY/CT OR PASSIVAT##########
L9          137     S       (OXIDE OR INSULAT###### OR DIELEC#######)(3A)(DIRECTLY OR IMMEDIATELY)(4A)SUBSTRATE
L10       10929     S       (OXIDE OR INSULAT###### OR DIELEC#######)(1A)(INITIAL OR FIRST OR BOTTOM OR LOWER OR
LOWEST OR BELOW)
L11      213501     S       (OXIDE OR INSULAT###### OR DIELEC#######)(1A)(FILM OR LAYER)
L12        3827     S       DIRECTLY(4A)SUBSTRATE
                    E OXIDES/CT

     FILE 'REGISTRY' ENTERED AT 15:21:03 ON 12 AUG 2004
L14       24489     S       O.SI/MF OR O SI/ELF OR SILICA
L15         396     S       N.O.SI/MF OR N O SI/ELF
                    E N4 SI3/MF
L16           3     S       "N4 SI3"/MF
L17         374     S       N.SI/MF OR N SI/ELEF
L18         821     S       L17 OR L16 OR N SI/ELF
                    E POLYIMID/PCT
L19       56064     S       (POLYIMIDE/PCT OR "POLYIMIDE FORMED"/PCT)
                    OR POLYIMIDE OR ((IMIDE OR IMIDO) AND (POLY OR POLYMER OR
                    MONOMER OR COPOLYMER OR HOMOPOLYMER))

     FILE 'HCAPLUS' ENTERED AT 15:25:50 ON 12 AUG 2004
L20      198369     S       L7 OR TREAT######(2A)SURFACE OR MODIF#######(2A)SURFACE OR (TREAT##### OR
EXPOS######)(4A)GAS OR GAS(4A)SURFACE
L21        9894     S       TRILAYER##### OR (TRI OR TRIPLE)(W)LAYER#### OR DISTINGUISH####(2A)LAYER OR
SEPARATE(2A)LAYER
L22        2593     S       L21 AND (STACK####### OR SANDWICH##### OR LAMINA####### OR MULTIL? OR (MULTI OR
MULTIPLE OR THIRD)(2W)(LAYER OR FILM))

     FILE 'REGISTRY' ENTERED AT 15:28:41 ON 12 AUG 2004
L23         245     S       OZONE OR O3/MF OR O2/MF OR O/MF
L24          68     S       N2/MF OR N/MF OR NITROGEN/CN
L25        5564     S       AMMONIA
L26        2707     S       ARGON

     FILE 'HCAPLUS' ENTERED AT 15:29:43 ON 12 AUG 2004
L27       59394     S       (L23 OR L24 OR L25 OR L26)(L)GAS
L28        8277     S       (L23 OR L24 OR L25 OR L26)(L)(VAPOR OR VAPOUR)
L29       27850     S       (L23 OR L24 OR L25 OR L26)(L)SURFACE
L30       35884     S       (L23 OR L24 OR L25 OR L26)(L)(TREAT######
                    OR MODIF##########)
L31       38851     S       (L23 OR L24 OR L25 OR L26)(L)(LAYER OR
                    FILM)
L32         334     S       (L27 OR L28) AND L29 AND L30
L33         295     S       (L27 OR L28) AND L29 AND L31
L34         251     S       (L27 OR L28) AND L30 AND L31
L35           1     S       L2
L36                 SEL PLU=ON  L35 1- IC :        2 TERMS
L37                 SEL PLU=ON  L35 1- RN :        9 TERMS
                    E INTEGRATED CIRCUITS/CT
L38      226887     S       "INTEGRATED CIRCUITS"/CT OR ("MONOLITHIC MICROWAVE INTEGRATED CIRCUITS"/CT OR
"OPTICAL INSTRUMENTS (L)CIRCUITS, INTEGRATED"/CT OR "OPTICAL INSTRUMENTS (L) INTEGRATED CIRCUITS"/CT OR "OPTICAL
INTEGRATED CIRCUITS"/CT OR "OPTICS (L) INTEGRATED"/CT OR "ELECTRONIC PACKAGES"/CT OR MICROELECTRONICS/CT OR
"MOLECULAR ELECTRONICS"/CT OR "PRINTED CIRCUITS"/CT) OR "SEMICONDUCTOR DEVICES"/CT OR IC OR ICS OR
CIRCUIT(L)INTEGRATED OR CSP OR SOI OR ELECTRIC CIRCUIT
L39        6477     S       L8 AND (L38 OR H01L?/IC)
L40         426     S       (L9 OR L10 OR L11) AND L12
L41           5     S       L39 AND L40
L42           7     S       (L39 OR L40) AND L7
L43        6480     S       (L39 OR L40) AND L8
L44         108     S       (L39 OR L40) AND L9
L45          95     S       (L39 OR L40) AND L10
L46        2584     S       (L39 OR L40) AND L11
L47         432     S       (L39 OR L40) AND L12
L48           0     S       (L39 OR L40) AND L13
L49         587     S       L14 AND L15 AND (L16 OR L17 OR L18)
L50           2     S       L49 AND L19
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L51          15     S      L50 OR (L49 AND (POLYIMID### OR (IMIDE##
                 OR IMIDO##)(2A)(POLY OR POLYMER OR SOFT OR PHOTO OR PHOTORESIST
                  OR PHOTOMASK OR LIGHT OR ?DEVELOP? OR PHOTODEFIN####### OR DEFIN#####)))
L52           0     S      L49 AND L12
L53          11     S      L49 AND L20
L54           1     S      L49 AND L21
L55           0     S      L49 AND L22
L56         136     S      L49 AND (L23 OR L24 OR L25 OR L26)
L57          14     S      L56 AND L27
L58           3     S      L56 AND GAS(5A)SURFACE
L59          36     S      L20 AND L21 AND L22
L60           0     S      L59 AND PASSIVAT########
L61          10     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND PASSIVAT########
L62           2     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND REACTIVITY
L63          25     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND SUSCEPT##########
L64           0     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND NONREACT?
L65           5     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND UNREACT?
L66           1     S      ((L20 AND (L21 OR L22)) OR (L21 AND L22)) AND NON REACT##########
L67        4210     S      (L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR
                 L44 OR L45 OR L46 OR L47 OR L48 OR L49 OR L50 OR L51 OR L52 OR
                 L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59) AND DIRECTLY
L68          751     S      (L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR
                 L44 OR L45 OR L46 OR L47 OR L48 OR L49 OR L50 OR L51 OR L52 OR
                 L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59) AND DIRECTLY(6A)SUBSTRATE
L69           53     S      (L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR
                 L44 OR L45 OR L46 OR L47 OR L48 OR L49 OR L50 OR L51 OR L52 OR
                 L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59) AND IMMEDIATE###(6A)SUBSTRATE
L70        2140     S      (L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR
                 L44 OR L45 OR L46 OR L47 OR L48 OR L49 OR L50 OR L51 OR L52 OR
                 L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59) AND (OXIDE OR
                 SIO OR SIO2 OR INSULAT#####)(3A)(COAT######## OR DEPOSIT#########)(6A)SUBSTRATE
L71          961     S      (L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR
                 L44 OR L45 OR L46 OR L47 OR L48 OR L49 OR L50 OR L51 OR L52 OR
                 L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59) AND (OXIDE OR
                 SIO OR SIO2 OR INSULAT#####)(2A)(COAT######## OR DEPOSIT#########)(2A)SUBSTRATE
L72           40     S      L71 AND PASSIVAT##########
L73          527     S      (L7 OR L8 OR L9 OR L10 OR L11 OR L12) AND
                 (L14 OR L15 OR L16 OR L17 OR L18 OR L19) AND (L20 OR L21 OR
                 L22) AND (L23 OR L24 OR L25)
L74          251     S      L73 AND OXIDE(3A)(COAT##### OR LAYER####
                 OR FILM##### OR INSULAT##### OR DIELEC######)
L75           36     S      L73 AND OXIDE(3A)SUBSTRATE
L76           34     S      L74 AND L75
L77            3     S      (L74 OR L75) AND DIRECTLY
L78            0     S      L73 AND OXIDE(3A)FIRST LAYER
L79            2     S      L73 AND OXIDE(3A)FIRST
L80            0     S      L73 AND OXIDE(3A)BOTTOM
L81            5     S      L73 AND OXIDE(3A)LOWER
L82        15911     S      (L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR
                 L13) AND (BOND###(3A)(LAYER#### OR FILM) OR (ADHE########### OR GLUE##### OR GLUING))

     FILE 'REGISTRY' ENTERED AT 15:52:25 ON 12 AUG 2004
L83         2707     S      ARGON


     FILE 'HCAPLUS' ENTERED AT 15:53:45 ON 12 AUG 2004
L84           49     S      L82 AND SECOND AND THIRD
L85          251     S      L82 AND L83
L86      1116175     S      L37
L87         3396     S      L82 AND L86
L88         8041     S      L36
L89          135     S      L82 AND L88
L90         1491     S      L82 AND INTERFAC########
L91         7450     S      L82 AND SURFACE
L92         1803     S      L18(L)(HARD OR PASSIVAT#######)
L93           50     S      L15(L)(ADHE######## OR GLUE##### OR GLUING OR BOND####)
L94           53     S      SECOND(W)PASSIVAT##########
L95         2278     S      PASSIVAT######(W)(FILMS OR LAYERS)
L96         2663     S      COMMON(2A)ELEMENT
L97          227     S      L82 AND (L92 OR L93 OR L94 OR L95 OR L96)
L98          220     S      L97 AND PASSIVAT########
L99           12     S      L97 AND DIRECTLY
L100          87     S      L97 AND SUBSTRATE
L101          80     S      L97 AND OXIDE
L102          30     S      L100 AND L101
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L103       1000     S      L9 OR (L41 OR L42) OR (L44 OR L45) OR (L50
                    OR L51 OR L52 OR L53 OR L54 OR L55 OR L56 OR L57 OR L58 OR L59
                    OR L60 OR L61 OR L62 OR L63 OR L64 OR L65 OR L66) OR L69 OR
                    L72 OR (L75 OR L76 OR L77 OR L78 OR L79 OR L80 OR L81) OR L84
                    OR L89 OR (L93 OR L94) OR (L99 OR L100 OR L101 OR L102)
L104        167     S      L103 AND DIRECTLY
L105         69     S      L103 AND IMMEDIATE##
L106        605     S      L103 AND SUBSTRATE
L107         75     S      L103 AND (MODIF########## OR TREAT######)(3A)SURFACE
L108        211     S      (L104 OR L105) AND L106
L109          4     S      L107 AND L108
L110        658     S      L103 AND (L104 OR L105 OR L106 OR L107 OR L108 OR L109)
L111        239     S      L110 AND PASSIVAT#########
L112        471     S      L110 AND (IC OR ICS OR INTEGRATED OR CIRCUIT OR SEMICONDUCT###### OR H01L?/IC)
L113        192     S      L111 AND L112
L114         65     S      (L94 OR L95) AND L113
L115          3     S      (L20 OR L21 OR L22) AND L114
L116        187     S      (L111 OR L112) AND (ADHE####### OR GLU####### OR BOND####(2A)(LAYER OR FILM))
L117          6     S      L116 AND OXIDE(5A)SUBSTRATE
L118        329     S      (L85 OR (L97 OR L98) OR (L104 OR L105 OR
                    L106 OR L107 OR L108 OR L109 OR L110 OR L111 OR L112 OR L113
                    OR L114 OR L115 OR L116) OR L103 OR (L32 OR L33 OR L34)) AND PASSIVAT#########/TI,IT,ST
L119         19     S      (L104 OR L105) AND L118
L120         19     S      L119 NOT (L109 OR  L117 OR L115)
L121          9     S      L120 AND ((L14 OR L15 OR L16 OR L17 OR L18
                    OR L19) OR (L23 OR L24 OR L25 OR L26) OR L83 OR ARGON OR GAS(3A)SURFACE)
L122          2     S      L14 AND L15 AND L18 AND L19
L123        138     S      L14 AND L15 AND L18 AND ((L23 OR L24 OR
                    L25 OR L26) OR ARGON)
L124          9     S      L123 AND (DIRECTLY OR PASSIVAT#######)
L125          4     S      L123 AND (GLU####### OR ADHE########)
L126         13     S      (L124 OR L125)
L127         24     S      (L121 OR L122) OR (L109 OR L117 OR L115)
L128         12     S      L126 NOT L127
L129         92     S      L14 AND (L15 OR L18 OR L19) AND PASSIVAT###
                    ##### AND (GAS(4A)SURFACE OR (L23 AND L24) OR (L23 AND L25) OR
                    (L23 AND L26) OR (L24 AND L25) OR (L24 AND L26) OR (L25 AND L26))
L130         36     S      L126 OR L127
L131         89     S      L129 NOT L130
L132         89     S      L131 AND PASSIVAT#########
L133       8041     S      L36
L134          7     S      L132 AND L133
L135    1116175     S      L37
L136          6     S      H01L023-58?/IC AND OXIDE AND PASSIVAT########
L137          0     S      H01L023-58?/IC AND OXIDE AND (TRI OR
                    TRIPLE OR 3 OR THREE)(W)LAYER#######
L138         50     S      PASSIVAT######## AND OXIDE AND (TRI OR
                    TRIPLE OR 3 OR THREE)(W)LAYER#######
L139          6     S      PASSIVAT######## AND OXIDE AND TRILAYER######
L140         29     S      (L138 OR L139) AND (IC OR ICS OR CIRCUIT OR INTEGRATED OR H01L?/IC)
L141          0     S      L140 AND (COMMON OR DIRECTLY OR IMMEDIATE##
                    )
L142          5     S      L140 AND SUBSTRATE(4A)(OXIDE OR INSULAT####
                    ## OR DIELEC###### OR SIO OR SIO2 OR DIOXIDE OR SILICA)
L143          0     S      L132 AND (L138 OR L139)
L144         36     S      (L126 OR L127)
L145         22     S      (L134 OR L136 OR L139 OR L142) NOT L144
L146          2     S      L145 AND GAS
L147          4     S      L145 AND SURFACE
L148          4     S      L147 NOT L146
L149         63     S      L19(L)PASSIVAT########
L150       3106     S      L19(L)(PHOTO OR LIGHT OR DEVELOP? OR PHOTOD? OR PHOTO##########)
L151          9     S      L149 AND L150
L152         80     S      (SECOND OR TWO OR 2)(1W)PASSIVAT#######(1W)
                    (LAYER#### OR FILM OR COAT##### OR SUBLAYER######)
L153          9     S      (L19 OR POLYIMIDE OR IMIDE) AND L152
L154          9     S      L153 NOT L151
```

12aug04 15:26:09 User259284 Session D2866.2

SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2004/Aug W01
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040805,UT=20040729
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	13623	DIRECTLY(4N)SUBSTRATE??
S2	3843	(IMMEDIATE?? OR BARE)(4N)SUBSTRATE??
S3	14885	(OXIDE OR INSULAT????? OR OXIDES OR DIOXIDE?? OR SIO2 OR SIO OR SILICA)(5N)SUBSTRATE??/TI,AB,CM
S4	488	S3 AND PASSIVAT??????????/TI,CM,AB
S5	117	S4 AND (IC OR ICS OR INTEGRATED(3N)CIRCUIT??? OR SOI OR CSP OR CHIPSCALE?? OR CHIP()SCALE?? OR MCM OR MCMS OR MULTICHIP??)/TI,AB,CM
S6	5	S5 AND (TRILAYER? OR (TRI OR THREE OR 3)(1W)(LAYER????? OR FILM? ? OR STACK????? OR SANDWICH??????))/TI,AB,CM
S7	244	(SECOND OR 2 OR TWO)(W)PASSIVAT??????(W)(LAYER?? OR FILM?? OR COAT?????)
S8	47	7AND1
S9	8	7AND2
S10	66	7AND3
S11	13	8AND10
S12	57	S8:S11 AND IC=H01L?
S13	1	8AND9
S14	5	9AND10
S15	8	S9 OR S13 OR S14
S16	8	S15 NOT S6
S17	8	S1:S5 AND S16

INSPEC on DIALOG 8/12/2004

Set	Items	Description
S1	3399	PASSIVAT??????(2N)(FILM?? OR LAYER????? OR COAT?????? OR MULTI OR MULTIPLE OR TWO OR SECOND OR SUBLAYER??)
S2	25019	'PASSIVATION' OR 'PROTECTIVE COATINGS' OR 'CORROSION PROTECTIVE COATINGS'
S3	25454	S1:S2
S4	605	(DIRECT?? OR IMMEDIATE?? OR BARE)(2W)SUBSTRATE
S5	14	3AND4
S6	2	S5 AND SURFACE??(3N)(OXIDE?? OR SIO OR DIOXIDE?? OR SILICA OR SIO2)
S7	3	S5 AND CI=N
S8	4	S5 AND CI=O
S9	0	S5 AND CI=AR
S10	6	S7:S8 NOT S6
S11	3	S10/1999-2004
S12	3	S10 NOT S11
S13	15313	S1:S2 AND PASSIVAT??????????
S14	2	4AND13
S15	1963	(DIRECT?? OR IMMEDIATE?? OR BARE)(4N)SUBSTRATE
S16	17	13AND15
S17	6	S16 AND CI=O
S18	1	S16 AND CI=N
S19	0	S16 AND CI=AR
S20	6	S17:S18
S21	332	S13 AND SUBSTRATE AND OXIDE
S22	207	S21 AND SURFACE
S23	13	S22 AND ADHE???????
S24	0	S22 AND GLU??????
S25	4	S23/1999-2004
S26	9	S23 NOT S25

129230

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 8/6/04 Serial # 10/013,103 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2829 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need. Need before 8/16 8/17

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

13-06-04 A 11:59 P

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ____
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 17-29

Problem: See pages 2 & 3
Solution: " " "

Please look for the materials that are disclosed.

Staff Use Only
Searcher: HARRISON
Searcher Phone: 22511
Searcher Location: STIC-EIC2800, JEF-4B68
Date Searcher Picked Up: 8-11
Date Completed: 8-12-04
Searcher Prep/Rev Time: 90
Online Time: 75

Type of Search
Structure (#)_____
Bibliographic X
Litigation_____
Fulltext X
Patent Family_____
Other_____

Vendors
STN_____
Dialog X
Questel/Orbit_____
Lexis-Nexis_____
WWW/Internet
Other

L146 **ANSWER** 2 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 1999:783447 HCAPLUS Full-text
DN 132:17954
ED Entered STN: 10 Dec 1999
TI **Fabrication of semiconductor devices by plasma CVD of silicon nitride passivation film**
IN Miyanaga, Takashi
PA Sony Corp., Japan

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11340223	**A2**	**19991210**	**JP 1998-141302**	**19980522**
PRAI JP 1998-141302		**19980522**		

AB The plasma CVD of a Si nitride **passivation** film over a circuit layer on a semiconductor substrate in the title fabrication employs CVD **gases** including Si nitride-forming reactants and a halo compound **gas** for involving simultaneous process by vapor depositing of a Si3N4 film with the Si nitride-forming reactants and etching of a portion of the depositing Si3N4 film with the halo compound **gas**. The halo compound may be CF4, C2F6, NF3, SF6, CHF3, or ClF3. The Si nitride-forming reactants may be SiH4, NH3, and/or N2. The simultaneous process gives depositing the Si3N4 **passivation** film an improved coating step coverage for ensuring semiconductor device reliability.

IT **Passivation**
(film deposition; fabrication of semiconductor devices by plasma CVD of silicon nitride **passivation** film)

IT **7783-54-2**, Nitrogen fluoride (NF3)
(fabrication of semiconductor devices by plasma CVD of silicon nitride **passivation** film)

RN 7783-54-2 HCAPLUS
CN Nitrogen fluoride (NF3) (6CI, 8CI, 9CI) (CA INDEX NAME)

IT **7664-41-7**, Ammonia, reactions **7727-37-9**, Nitrogen, reactions **7803-62-5**, Silicon hydride (SiH4), reactions
(fabrication of semiconductor devices by plasma CVD of silicon nitride **passivation** film)

RN 7664-41-7 HCAPLUS
CN Ammonia (8CI, 9CI) (CA INDEX NAME)

RN 7727-37-9 HCAPLUS
CN Nitrogen (8CI, 9CI) (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (8CI, 9CI) (CA INDEX NAME)

IT **12033-89-5P**, Silicon nitride (Si3N4), properties
(**passivation** film, CVD-etching; fabrication of semiconductor devices by plasma CVD of silicon nitride **passivation** film)

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L148 **ANSWER** 3 OF 4 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:909273 HCAPLUS Full-text
DN 134:65011
ED Entered STN: 28 Dec 2000
TI Integration of low-K SiOF as interlayer dielectric for Al-gapfill application
IN Huang, Richard J.; Iacoponi, John A.
PA Advanced Micro Devices, Inc., USA

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6166427	**A**	**20001226**	**US 1998-231649**	**19980115**
PRAI US 1998-231649		**19980115**		

AB A method for producing a dielec. layer in a semiconductor product includes two steps. The 1st step is forming a fluorinated layer (e.g. SiOF or fluorosilicate glass (FSG)) which includes a material formed in part with F. The 2nd step is forming a fill layer (e.g. SiO2) above the fluorinated layer. The fill layer is substantially free of materials formed in part with F. A top **surface** of the fill layer can be planarized. **Surface** treatments and **oxide** caps can be applied to the planarized **surface** to form F barriers if part of the fluorinated layer is exposed to higher layers. Such a method, and a semiconductor device or integrated circuit manufactured allow the dielec. constant of an inter-layer dielec. (ILD) to be lowered while also minimizing the complexity and expense of the manufacturing process.

IT Dielectric films
Integrated circuits
Passivation

L128 **ANSWER** 7 OF 12 **HCAPLUS COPYRIGHT ACS on STN**
AN 1999:731769 HCAPLUS Full-text
DN 131:331116
ED Entered STN: 17 Nov 1999
TI Reducing bonding pad loss in integrated circuits using a capping layer when etching bonding pad **passivation** openings
IN Hsiao, Yung-Kuan; Wu, Cheng-Ming; Lee, Yu-Hua
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**US 5985765**	**A**	**19991116**	**US 1998-75368**	**19980511**
PRAI	**US 1998-75368**		**19980511**		

AB Bonding pad loss is reduced by using a capping layer when contact openings are etched to the bonding pads, while concurrently etching much deeper fuse openings to the substrate. Bonding pads are used on the top surface of integrated circuit semiconductor chips to provide external elec. connections for I/O and power. Fuses are used in the underlying insulating layers to remove redundant defective circuit elements and thereby repair defective chips. It is desirable (cost effective) to etch the contact openings in the **passivation** layer to the bonding pads near the top surface on the chip and to concurrently etch the much deeper fuse openings in the thick underlying insulating layers over the fuses. However, because of the difference in etch depth of the 2 types of openings, the bonding pads composed of Al/Cu are generally overetched, causing bond-pad reliability problems. This invention uses a novel process in which a capping layer, having a low etch rate, is formed on the bonding pads to prevent overetching while the fuse openings are etched to the desired depth in the thicker insulating layers.

IT **Passivation**
(reducing bonding pad loss in integrated circuits using a capping layer when etching openings for bonding pads in **passivation** layers)

IT 12033-89-5, Silicon nitride, processes 132614-63-2, Silicon nitride oxide (Si(N,O))
(reducing bonding pad loss in integrated circuits using a capping layer when etching openings for bonding pads in **passivation** layers containing)

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

RN 132614-63-2 HCAPLUS
CN Silicon nitride oxide (Si(N,O)) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0 - 1	17778-88-0
O	0 - 1	17778-80-2
Si	1	7440-21-3

IT **7440-37-1, Argon**, processes
(reducing bonding pad loss in integrated circuits using a capping layer when etching openings for bonding pads in **passivation** layers using gas mixts. containing)

RN 7440-37-1 HCAPLUS
CN Argon (8CI, 9CI) (CA INDEX NAME)

Ar

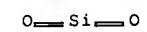
IT **7631-86-9**, Silica, processes
(reducing bonding pad loss using a capping layer when etching openings for bonding pads in integrated circuits containing)

RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L121 **ANSWER** 8 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1998:60766 HCAPLUS Full-text
DN 128:187436
ED Entered STN: 02 Feb 1998
TI **Plasma deposition of Si-N and Si-O passivation layers on three-dimensional sensor devices**
AU Schmid, P.; Orfert, M.; Vogt, M.
CS TU Dresden, Institut fur Halbleiter- und Mikrosystemtechnik, D-01062, Dresden, Germany
SO **Surface and Coatings Technology (1998), 98(1-3), 1510-1517**
CODEN: SCTEEJ; ISSN: 0257-8972
PB Elsevier Science S.A.
DT Journal
LA English
CC 76-14 (Electric Phenomena)
AB In sensor fabrication particularly high demands are made on the **passivation layers**, since the active sensor area is exposed **directly** to the environment. Typical requirements on **passivation layers** are high elec. resistance, high d. against moisture penetration, good **adhesion** and low mech. stress. In earlier works planar sensors have been successfully **passivated** by plasma-enhanced chemical vapor-deposited (PECVD) SiO and SiN layers. However, many sensor devices are not available in planar techniques, but as three-dimensional (3D) devices. The object of this work was to develop a PECVD **passivation** technique for such 3D sensor devices. For the exptl. work an electron cyclotron resonance (ECR) plasma reactor was used to deposit **passivation layers** on model **substrates**. Deposition rate and layer quality were measured at various **substrate** locations, orientations and temps. The layer quality was determined by ellipsometer data, IR spectra, SEM and moisture diffusion expts. As result of these investigations the following tendencies could be established. The deposition rate increases in the z-direction (height) by 30% cm-1. At low deposition pressure (0.66-1.33 Pa) the deposition rate depends strongly on the **substrate** orientation, i.e. it decreases from top to side by .apprx.50% and is even lower on the bottom side. Narrow structures with line widths of 1.3 mm and aspect ratios <1 could be well **passivated**. However, narrow undercuts with aspect ratios »1 could not be **passivated** sufficiently. At higher deposition pressures (20.35 Pa), more homogeneous film deposition in gaps and a significantly better coating of bond wires could be achieved.

IT (plasma deposition of Si-N and Si-O **passivation layers** on three-dimensional sensor devices)
RN 7631-86-9 HCAPLUS
CN **Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)**



RN 12033-89-5 HCAPLUS
CN **Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)**

IT **7664-41-7, Ammonia, reactions 7727-37-9, Nitrogen, reactions 7782-44-7, Oxygen, reactions 7803-62-5, Silane, reactions**
(plasma deposition of Si-N and Si-O **passivation layers** on three-dimensional sensor devices)
RN 7664-41-7 HCAPLUS
CN **Ammonia (8CI, 9CI) (CA INDEX NAME)**

RN 7727-37-9 HCAPLUS
CN Nitrogen (8CI, 9CI) (CA INDEX NAME)

RN 7782-44-7 HCAPLUS
CN Oxygen (8CI, 9CI) (CA INDEX NAME)

L154 **ANSWER** 2 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:219098 HCAPLUS Full-text
DN 132:244981
ED Entered STN: 05 Apr 2000
TI **Passivation technology combining improved adhesion in passivation and a scribe street without passivation in semiconductor device fabrication**
IN Dass, M. Lawrence A.; Seshan, Krishna; Gaeta, Isaura
PA Intel Corporation, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**US 6046101**	**A**	**20000404**	**US 1997-1970**	**19971231**
PRAI	**US 1997-1970**		**19971231**		

AB An integrated circuit passivation layer including a first passivation layer portion of silicon nitride treated with nitrous oxide and a **second passivation layer** portion of **polyimide**. Also, a method of passivating an integrated circuit wafer including depositing a first passivation layer over the top surface of an integrated circuit wafer having a scribe street area between adjacent integrated circuit device portions, depositing a **second passivation layer** over the first passivation layer, and patterning the first passivation layer and the **second passivation layer** to expose the scribe street area.

IT **Polyimides**, uses
(passivation technol. combining improved adhesion in passivation and a scribe street without passivation in semiconductor device fabrication)

L128 **ANSWER** 8 OF 12 **HCAPLUS COPYRIGHT ACS on STN**
AN 1999:686634 HCAPLUS Full-text
DN 131:294446
ED Entered STN: 28 Oct 1999
TI **Forming integrated circuit capacitor structures and reducing parasitic capacitance in them**
IN Visokay, Mark R.; Colombo, Luigi; Mcintyre, Paul; Summerfelt, Scott R.
PA Texas Instruments Incorporated, USA

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5972722	**A**	**19991026**	**US 1998-60152**	**19980414**
PRAI US 1997-42982P	**P**	**19970414**		

AB A high-k dielec. capacitor structure and fabrication method incorporate an **adhesion**-promoting etch stop layer to promote **adhesion** of the bottom electrode to the interlevel dielec. layer and to provide a well controlled, repeatable and uniform recess prior to the dielec. deposition. By using a sacrificial layer, e.g. Si3N4, this layer can act as an etch stop during the recess etch to eliminate parasitic capacitance between adjacent capacitor cells and can promote **adhesion** of the bottom electrode material to the substrate.
IT Vapor deposition process
(chemical; of **adhesion**-promoting sacrificial etch stop layers in integrated circuit capacitor structures)
IT 7631-86-9, Silica, processes 7631-86-9D, Silica, silicon-excess, processes 12033-89-5, Silicon nitride, processes 132614-63-2, Silicon nitride oxide (Si(N,O)) 246227-27-0, Silicon nitride (SiN0.5-1.34)
(**adhesion**-promoting sacrificial etch stop layer in integrated circuit capacitor structures)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

RN 132614-63-2 HCAPLUS
CN Silicon nitride oxide (Si(N,O)) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0 - 1	17778-88-0
O	0 - 1	17778-80-2
Si	1	7440-21-3

RN 246227-27-0 HCAPLUS
CN Silicon nitride (SiN0.5-1.34) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	0.5 - 1.34	17778-88-0
Si	1	7440-21-3

IT 7440-37-1, Argon, processes 7782-44-7, Oxygen, processes
(etching by; of integrated circuit capacitor bottom electrodes)
RN 7440-37-1 HCAPLUS
CN Argon (8CI, 9CI) (CA INDEX NAME)

Ar

RN 7782-44-7 HCAPLUS
CN Oxygen (8CI, 9CI) (CA INDEX NAME)

26/9/1
DIALOG(R)File 2:INSPEC

6046657 INSPEC Abstract Number: B9811-2530D-027
Title: **Adhesion** enhancement at Co(P) diffusion barrier/polyimide interfaces
Author(s): O'Sullivan, E.J.; Schrott, A.G.; Sambucetti, C.J.; Kaja, S.; Semkow, K.W.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: Proceedings of the Symposium on Interconnect and Contact Metallization p.173-81
Editor(s): Rathore, H.S.; Mathad, G.S.; Plougonven, C.; Schuckert, C.C.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1998 Country of Publication: USA viii+275 pp.
ISBN: 1 56677 184 6 Material Identity Number: XX98-01017
Conference Title: Proceedings of the Symposium on Interconnect and Contact Metallization
Conference Sponsor: Electrochem. Soc
Conference Date: 31 Aug.-5 Sept. 1997 Conference Location: Paris,
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: We studied the **adhesion** of polyimide to electrolessly deposited Co(P) **films** used as **passivation** of Cu lines in multilayer thin film packages. For best **adhesion**, it was necessary to grow a thin **oxide** film (<or=60 AA thick) on the Co(P) **surface** prior to PI application. **Oxide** films with the desired properties were produced in a well controlled fashion by immersion in a mildly oxidizing borate solution. The **oxide** thickness and the valency states of Co were investigated ex-situ by means of X-ray photoelectron spectroscopy (XPS). The **oxide** thickness and the relative abundance of Co/sup 3+/ varied with the pH of the solution. Peel tests (90 degrees) were correlated with XPS analysis of the uncovered **substrate** and the back of the peeled PI. The results indicated that the interaction of the **adhesion** promoter with the **surface** varied with the **oxide** chemistry, and that the preferred films were Co/sup 3+/ rich. (10 Refs)
Subfile: B
Descriptors: **adhesion**; chemical interdiffusion; cobalt compounds; diffusion barriers; integrated circuit interconnections; integrated circuit metallisation; integrated circuit reliability; interface structure; mechanical testing; oxidation; **passivation**; polymer films; **surface** chemistry; valency; X-ray photoelectron spectra

20/9/4
DIALOG(R)File 2:INSPEC

6053589 INSPEC Abstract Number: B9811-2560R-073
Title: Demonstration of enhancement-mode p-channel GaAs MOSFETs with Ga/sub 2/O/sub 3/(Gd/sub 2/O/sub 3/) **passivation**
Author(s): Ren, F.; Hong, M.; Hobson, W.S.; Kuo, J.M.; Lothian, J.R.; Mannaerts, J.P.; Kwo, J.; Chu, S.N.G.; Chen, Y.K.; Cho, A.Y.
Author Affiliation: Lucent Technol., Bell Labs., Murray Hill, NJ, USA
Conference Title: Proceedings of the Twenty-Sixth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXVI) p.84-90
Editor(s): Buckley, D.N.; Chu, S.N.G.; Hou, H.Q.; Sah, R.E.; Vilcot, J.P. ; Deen, M.J.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA ix+322 pp.
ISBN: 1 56677 128 5 Material Identity Number: XX98-00791
Conference Title: Proceedings of the Twenty-Sixth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXVI)
Conference Sponsor: Electrochem. Soc
Conference Date: 4-9 May 1997 Conference Location: Montreal, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: We report on the first demonstration of an enhancement-mode p-channel GaAs metal oxide semiconductor field effect transistor (MOSFET) **directly** on GaAs semi-insulating **substrate** with a high quality Ga/sub 2/O/sub 3/(Gd/sub 2/O/sub 3/) material as the gate dielectric and ion-implant technology. Ga/sub 2/O/sub 3/(Gd/sub 2/O/sub 3/) was electron beam deposited from a high purity single crystal Ga/sub 2/Gd/sub 5/O/sub 12/ source. The dielectric constant and breakdown field of Ga/sub 2/O/sub 3/(Gd/sub 2/O/sub 3/) are 14.2 and 3.6 MV/cm, respectively. The source and drain regions were selectively implanted with Zn for low resistance ohmic contacts. AuBe/Pt/Au and Ti/Pt/Au were then deposited for p-ohmic contact and gate electrode, respectively. The device, with a 40*50 mu m/sup 2/ gate geometry, exhibits a threshold of -0.6 V, an extrinsic transconductance of 0.3 mS/mm and an excellent gate breakdown field greater than 3 MV/cm. (8 Refs)
Subfile: B
Descriptors: electric breakdown; electron beam deposition; gadolinium compounds; gallium arsenide; gallium compounds; III-V semiconductors; ion implantation; MOSFET; ohmic contacts; **passivation**; permittivity

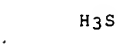
L146 **ANSWER** 1 OF 2 **HCAPLUS COPYRIGHT ACS on STN**
AN 2000:416633 HCAPLUS Full-text
DN 133:25416
ED Entered STN: 22 Jun 2000
TI Method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**
IN Detar, Mark A.
PA Motorola Inc., USA

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6077791	**A**	**20000620**	**US 1998-38466**	**19980311**
PRAI US 1996-771352	**A2**	**19961216**		

AB Deuterated compds. were used to form **passivation** (20) and other insulating layers to reduce the H content within those films. Semiconductor source **gases**, nitride source **gases**, and dopant **gases** can be obtained in deuterated form. Process steps for forming and etching are substantially the same as those used to form and etch conventional insulating layer. A sintering step can be performed using deuterated **gas** or omitted altogether.

IT Vapor deposition process
(chemical; method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**)
IT Dielectric films
Passivation
IT **Gases**
(sintering; method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**)
IT **12033-89-5P**, Silicon nitride, processes
(method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

IT **1590-87-0D**, Disilane, deuterated
(method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**)
RN 1590-87-0 HCAPLUS
CN Disilane (6CI, 8CI, 9CI) (CA INDEX NAME)



IT **7727-37-9**, Nitrogen, uses **7727-37-9D**, Nitrogen, compds., uses **7782-44-7**, Oxygen, uses **10028-15-6**, Ozone, uses
(precursor; in method of forming **passivation** and insulating layers for semiconductor devices using deuterium-containing reaction **gases**)
RN 7727-37-9 HCAPLUS
CN Nitrogen (8CI, 9CI) (CA INDEX NAME)

RN 7782-44-7 HCAPLUS
CN Oxygen (8CI, 9CI) (CA INDEX NAME)

RN 10028-15-6 HCAPLUS
CN Ozone (8CI, 9CI) (CA INDEX NAME)

IT **13550-49-7**, Ammonia-d3 **13587-49-0**, Ammonia-d **13780-28-4**, Ammonia-d2

26/9/5
DIALOG(R)File 2:INSPEC

5258325 INSPEC Abstract Number: B9606-2550E-081
Title: Electrical properties of high-quality stacked CdTe/photo-enhanced native **oxide** for HgCdTe **passivation**
Author(s): Yan-Kuin Su; Chung-Te Lin; Hsin-Tien Huang; Shoou-Jinn Chang; Tai-Ping Sun; Gin-Shiang Chen; Jiunn-Jye Luo
Author Affiliation: Dept. of Electr. Eng., Nat. Cheng Kung Univ., Tainan, Taiwan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes (Japan) vol.35, no.2B p.1165-7
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: Feb. 1996 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199602)35:2BL.1165:EPHQ;1-G
Material Identity Number: C579-96005
Conference Title: 1995 International Conference on Solid State Devices and Materials (SSDM `95)
Conference Date: 21-24 Aug. 1995 Conference Location: Osaka, Japan
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: A novel **surface** treatment method for obtaining a high-quality CdTe/HgCdTe interface is proposed. By stacking photoenhanced native **oxide** and CdTe **films**, we successfully **passivated** HgCdTe. This technique is advantageous because photoenhanced native oxides can form an excellent interface and **adhere** to HgCdTe **substrate** well. Using this novel technique, we have fabricated metal/CdTe/photoenhanced native **oxide** /HgCdTe structured metal-insulator-semiconductor (MIS) capacitors. From capacitance-voltage (C-V) measurement, we found that the comparison, conventional metal/CdTe/HgCdTe structured MIS capacitors were also fabricated. We found that capacitors with the photoenhanced native **oxide** layer have a much lower leakage current. Such a marked leakage current reduction is due to the good interfacial properties between the photoenhanced native **oxide** and the HgCdTe **substrate**. (11 Refs)
Subfile: B
Descriptors: cadmium compounds; II-VI semiconductors; interface structure ; mercury compounds; MOS capacitors; oxidation; **passivation**; **surface** treatment

L154 **ANSWER** 4 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1998:277612 HCAPLUS Full-text
DN 128:328873
ED Entered STN: 14 May 1998
TI **Radiation imager with discontinuous dielectric**
IN Possin, George Edward; Liu, Jianqiang; Kwasnick, Robert Forrest
PA General Electric Company, USA

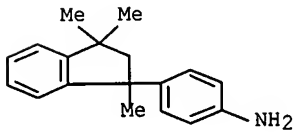
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 838860	A2	19980429	EP 1997-308466	19971023
	EP 838860	A3	19990414		
	US 5777355	**A**	**19980707**	**US 1996-772446**	**19961223**
	JP 10214954	A2	19980811	JP 1997-287500	19971021
PRAI	**US 1996-772446**		**19961023**		

AB Radiation imagers having a plurality of photosensitive elements has a **two-tier passivation layer** disposed between the top patterned common electrode contact layer and resp. photosensor islands. The top passivation layer is a polymer bridge member disposed between adjacent photodiodes so as to isolate defects such as moisture-induced leakage in any bridge island layer to the two adjacent photodiodes spanned by the bridge island.

IT **Polyimides**, uses
(radiation imager with discontinuous dielec.)
IT **62929-02-6**, Probromide 286
(radiation imager with discontinuous dielec.)
RN 62929-02-6 HCAPLUS
CN 1,3-Isobenzofurandione, 5,5'-carbonylbis-, polymer with 1(or 3)-(4-aminophenyl)-2,3-dihydro-1,3,3(or 1,1,3)-trimethyl-1H-inden-5-amine

CM 1

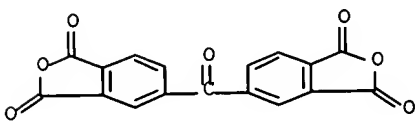
CRN 60451-10-7
CMF C18 H22 N2
CCI IDS



D1—NH_2

CM 2

CRN 2421-28-5
CMF C17 H6 O7



L154 **ANSWER** 5 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1998:219317 HCAPLUS Full-text
DN 128:277840
ED Entered STN: 18 Apr 1998
TI **Double mask hermetic passivation method providing enhanced resistance to moisture**
IN Bryant, Frank R.; Singh, Abha R.; Cunningham, James A.
PA SGS-Thomson Microelectronics, Inc., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**US 5736433**	**A**	**19980407**	**US 1996-778021**	**19961231**
	JP 10233454	**A2**	**19980902**	**JP 1997-353242**	**19971222**
PRAI	**US 1996-651618**		**19960522**		
	US 1996-738738		**19961028**		
	US 1996-778021		**19961231**		

AB A passivation structure is formed using **two passivation layers** and a protective overcoat layer using two masking steps. The first passivation layer is formed over the wafer and openings are provided to expose portions of the pads for testing the device and fusible links. After testing and laser repair, a **second passivation layer** is formed over the wafer followed a deposit of the protective overcoat. The protective overcoat is patterned and etched, exposing the pads. The remaining portions of the protective overcoat are used as a mask to remove portions of the **second passivation layer** overlying the pads. Leads are then attached to pads and the devices are encapsulated for packaging. The **second passivation layer** overlaps edge portions of the first passivation layer at the bond pads to enhance moisture resistance.

IT **Polyimides**, processes
(protective overcoat; double mask hermetic passivation method providing enhanced resistance to moisture)

IT **7631-86-9, Silicon dioxide, processes** **11105-01-4, Silicon oxynitride** **12033-89-5, Silicon nitride, processes**
(double mask hermetic passivation method providing enhanced resistance to moisture)

17/TI,PN,PD,AN,AD,IC,AB,AB,K/2 (Item 2 from file: 348)

METHOD OF MANUFACTURING A SEMICONDUCTOR THIN FILM TRANSISTOR

PATENT (CC, No, Kind, Date): EP 714140 A1 960529 (Basic)
EP 714140 A1 980401
EP 714140 B1 030903
WO 95034916 951221
APPLICATION (CC, No, Date): EP 95921972 950615; WO 95JP1196 950615
PRIORITY (CC, No, Date): JP 94133374 940615; JP 9572144 950329
INTERNATIONAL PATENT CLASS: H01L-021/205; G02F-001/136; H01L-021/336; H01L-021/20; C23C-016/24

ABSTRACT EP 714140 A1

In order to fabricate a high performance thin film semiconductor device using a low temperature process in which it is possible to use low price glass substrates, a thin film semiconductor device has been fabricated by forming a silicon film at less than 450(degree)C, and, after crystallization, keeping the maximum processing temperature at or below 350(degree)C.

In applying the present invention to the fabrication of an active matrix liquid crystal display, it is possible to both easily and reliably fabricate a large, high-quality liquid crystal display. Additionally, in applying the present invention to the fabrication of other electronic circuits as well, it is possible to both easily and reliably fabricate high-quality electronic circuits. (see image in original document)

...SPECIFICATION grown on the substrate in step four. The deposited layer functions as the underlevel protection layer on top of the substrate but functions as a **second passivation layer** on areas in the deposition chamber away from the substrate. Because the underlevel protection layer by itself is able to prevent the diffusion of impurities...SiO(sub 2) film was used as the gate insulator layer and was deposited to a thickness of 1200 A using PECVD. (Figure 1 (b)) **Immediately** prior to setting the **substrate** in the PECVD reactor, the substrate was soaked for 20 seconds in a 1.67% dilute hydrofluoric acid solution to remove the native oxide layer...

...SPECIFICATION grown on the substrate in step four. The deposited layer functions as the underlevel protection layer on top of the substrate but functions as a **second passivation layer** on areas in the deposition chamber away from the substrate. Because the underlevel protection layer by itself is able to prevent the diffusion of impurities ...1, a SiO2)) film was used as the gate insulator layer and was deposited to a thickness of 1200 A using PECVD. (Figure 1 (b)) **Immediately** prior to setting the **substrate** in the PECVD reactor, the substrate was soaked for 20 seconds in a 1.67% dilute hydrofluoric acid solution to remove the native oxide layer...

...CLAIMS an underlevel protection layer of an insulating material; and a field effect transistor having a semiconductor film formed upon said underlevel protection layer of the **substrate**, a gate **insulator** layer, and a gate electrode; and an electrically insulating interlevel insulator layer between the interconnects of said field effect transistor;

the formation of a **passivation** layer in said deposition chamber in step 2,

the setting of substrate(s) in said deposition chamber in step 3,

17/TI,PN,PD,AN,AD,IC,AB,AB,K/8 (Item 2 from file: 349)

CONSTRUCTIONS AND MANUFACTURING PROCESSES FOR THERMALLY ACTIVATED PRINT HEADS

Patent and Priority Information (Country, Number, Date):
Patent: WO 9632267 A1 19961017
Application: WO 96US4855 19960409 (PCT/WO US9604855)

English Abstract
A monolithic printing head having a nozzle configuration in which the heater element is formed using a self-aligned process, where the thickness of the heater, the width of the heater, and the position of the heater in relation to the nozzle are all determined by deposition and etching steps, instead of lithographic processes. In this manner, much greater control of these parameters can be achieved than is generally possible with lithographic processes. No mask is required for the heater. A print head configuration also provides reduced power requirements and incorporates: (1) the provision of a thermally insulating layer between the heater and the substrate; (2) minimizing the thermal mass of the heater and surrounding solid material; (3) minimizing the distance between the heater and the ink meniscus; (4) using a material of relatively high thermal conductivity to **passivate** the heater against corrosion by the ink; and (5) undercutting the substrate in the region of the heater. A method of manufacturing such a nozzle and heater configuration is disclosed.

Detailed Description
... incorporate drive circuitry, data distribution circuitry, and fault tolerance. Also, the active circuitry of the head is protected from chemical attack by the ink by **two passivation layers**: silicon nitride and tantalum

Claim

8. A drop on demand printing head as claimed in claim 7 wherein the layer of material between the heater and the **substrate** is silicon **dioxide**.

9. A drop on demand printing head as claimed in claim 1 further comprising:
(a) a plurality of drop-emitter nozzles;
(b) a body of...conductive coating overlying said heater.

19. The invention defined in claim 18 wherein said coating

20. The invention defined in claim 19 further comprising a **passivation** material layer intermediate said heater and said coating.

21. The invention defined in claim 19 wherein said **passivation** layer comprises a tantalum material.
22. A method of fabricating a printing head which includes a self-aligned heater comprising the steps of:
(a) forming...A drop on demand printing head as claimed in claim 31 wherein said actuator is situated on a rim protruding from the surface of said **substrate** in the **immediate** vicinity of said actuator.

33. A drop on demand printing head as claimed in claim 32 characterized in that the substrate material in the region...and the substrate.

37. A drop on demand printing head as claimed in claim 36 wherein the layer of material between the heater and the **substrate** is silicon **dioxide**.

38. A method of manufacture of a drop on demand printing head as claimed in claim 35 wherein the nozzle is formed by anisotropic etching...

L151 **ANSWER** 1 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1996:100848 HCAPLUS Full-text
DN 124:177278
ED Entered STN: 17 Feb 1996
TI **Polyimide precursors, photosensitive polymer compositions, and electronic devices prepared therefrom**
IN Okabe, Yoshiaki; Ishida, Mina; Miwa, Takao; Takahashi, Akio
PA Hitachi Ltd, Japan; Hitachi Chemical Co Ltd

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07304871	**A2**	**19951121**	**JP 1994-122020**	**19940512**
PRAI JP 1994-122020		**19940512**		

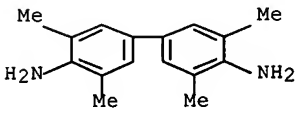
AB Title precursors comprise repeating units [A(CO2H)2(CONH)(CONHB)]n (A = 3,3',4,4'-biphenyltetrayl, p-terphenyl-3,3",4,4"-tetrayl, 1,2,4,5-benzenetetrayl; B = phenylene or biphenylene; R = C1-3 alkyl; n = 14-270) and photosensitive groups are incorporated to the precursors to give the compns. Thus, 3,3',4,4'-biphenyltetracarboxylic dianhydride and tetramethyl-1,4-phenylenediamine were treated in N-methylpyrrolidone to obtain a polyamic acid, 300 g of which was treated with 83.0 g glycidyl methacrylate at 60° for 48 h, and then mixed with 2.6 g 1-phenyl-3-ethoxypropanetrione 2-benzoyloxime and 2.4 g 4,4'-bis(diethylamino)benzophenone, applied on a Si wafer, UV irradiated at 365 nm through a photo mask, developed with choline hydroxide solution, rinsed, and treated at 350° for 30 min to form a polyimide pattern showing Tg 361°.

IT **127669-56-1DP**, reaction products with [[(dinitrobenzyl)oxy]carbonyl]cyclohexylamine **174061-93-9P 174061-94-0P 174061-95-1P 174061-96-2P 174061-97-3P**
(photoresists containing; polyimide precursors for manufacture of **photosensitive polyimides for passivation films**)

RN 127669-56-1 HCAPLUS
CN [5,5'-Biisobenzofuran]-1,1',3,3'-tetrone, polymer with 3,3',5,5'-tetramethyl[1,1'-biphenyl]-4,4'-diamine (9CI) (CA INDEX NAME)

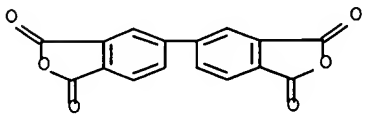
CM 1

CRN 54827-17-7
CMF C16 H20 N2



CM 2

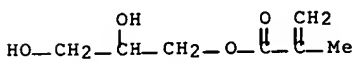
CRN 2420-87-3
CMF C16 H6 O6



RN 174061-93-9 HCAPLUS
CN [5,5'-Biisobenzofuran]-1,1',3,3'-tetrone, polymer with 2,3,5,6-tetramethyl-1,4-benzenediamine, 2-hydroxy-3-[(2-methyl-1-oxo-2-propenyl)oxy]propyl ester (9CI) (CA INDEX NAME)

CM 1

CRN 5919-74-4
CMF C7 H12 O4



L154 **ANSWER** 6 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1995:820759 HCAPLUS Full-text
DN 123:215940
ED Entered STN: 29 Sep 1995
TI **Manufacture apparatus of resin coatings in bevels of semiconductor devices**
IN Yamada, Osamu
PA Fuji Electric Co Ltd, Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 07147393**	**A2**	**19950606**	**JP 1994-41653**	**19940314**
	JP 3111794	B2	20001127		
PRAI	**JP 1993-178404**	**A**	**19930720**		
	JP 1993-242263	**A**	**19930929**		

AB After etching the bevel regions of a semiconductor substrate to remove the distorted layer, UV radiation using high pressure Hg lamp is applied when the **polyimide** resins (first passivation film) is spread with a contactless resin spreading apparatus, then the silicone resin (**second passivation film**) is used to mold the final shape. As the adhesion is stronger between the substrate and the first passivation film than between the **two passivation films**, the first passivation film will survive even there are cracks on the **second passivation film** due to the pressure on it.

IT **Polyimides**, processes
Siloxanes and Silicones, processes
(manufacture apparatus of resin coatings in bevels of semiconductor devices)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(manufacture apparatus of resin coatings in bevels of semiconductor devices)

L121 **ANSWER** 9 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1995:261571 HCAPLUS Full-text
DN 122:44303
ED Entered STN: 24 Dec 1994
TI Manufacture of **semiconductor** device with aluminum alloy wiring
IN Yamashita, Hiroshi
PA Matsushita Electronics Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM **H01L021-3205**
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06267949	**A2**	**19940922**	**JP 1993-53794**	**19930315**
PRAI JP 1993-53794		**19930315**		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 06267949	ICM	**H01L021-3205**

AB The title manufacture involves the following steps: (1) forming an interlayer **insulating film on a Si substrate directly** or via an elec. **insulating film**, (2) depositing an elec. conductive Al alloy film on the interlayer film by Ar sputtering with heating the **substrate** at 250-300°, (3) etching the elec. conductive film to form a wiring, (4) heating the wiring, (5) depositing a **passivation** film on the wiring, and (6) heating the **passivation** film. Electromigration resistance of Al wiring was improved.

IT **12033-89-5P**, Silicon nitride, uses
RL: DEV (Device component use); IMF (Industrial manufacture); PREP (Preparation); USES (Uses)
(**passivation** film, sputtering of; manufacture of **semiconductor** device with aluminum alloy wiring)

IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(**substrate**; manufacture of **semiconductor** device with aluminum alloy wiring)

IT 72893-14-2P
RL: DEV (Device component use); IMF (Industrial manufacture); PEP (Physical, engineering or chemical process); PREP (Preparation); PROC (Process); USES (Uses)
(wiring, sputtering and etching of; manufacture of **semiconductor** device with aluminum alloy wiring)

IT **12033-89-5P**, Silicon nitride, uses
RL: DEV (Device component use); IMF (Industrial manufacture); PREP (Preparation); USES (Uses)
(**passivation** film, sputtering of; manufacture of **semiconductor** device with aluminum alloy wiring)

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L154 **ANSWER** 7 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1995:283185 HCAPLUS Full-text
DN 122:44197
ED Entered STN: 10 Jan 1995
TI **Manufacture of compound semiconductor wafers**
IN Yoshimura, Kazunori; Nagayama, Hiroshi
PA Oki Electric Ind Co Ltd, Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 06151583**	**A2**	**19940531**	**JP 1992-296119**	**19921105**
PRAI	**JP 1992-296119**		**19921105**		

AB In manufacture of compound semiconductor wafers with passivation films covering devices and dicing lines for dividing chips, the dicing line structure comprises passivation films in two sides of the lines and an amorphous film between the **two passivation films** separated by channels to protect the passivation films from breaking and cracking. The amorphous film can be **polyimide** resin film or silicon nitride film. In the case of silicon nitride, at least one substrate area along the dicing line has a metal coating.

IT **Polyimides**, uses
(manufacture of compound semiconductor wafers with dicing line structure containing)
IT **12033-89-5, Silicon nitride, uses**
(manufacture of compound semiconductor wafers with dicing line structure containing)

L117 **ANSWER** 5 OF 6 **HCAPLUS COPYRIGHT ACS on STN**
AN 1994:196003 HCAPLUS Full-text
DN 120:196003
ED Entered STN: 16 Apr 1994
TI **Manufacture of photoelectric transfer devices for silicon solar cells**
IN Okamoto, Koji; Okuno, Tetsuhiro; Yokozawa, Juji; Moriuchi, Sota; Nakajima, Kazutaka
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM **H01L031-04**
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 05315628**	**A2**	**19931126**	**JP 1992-116232**	**19920508**
	JP 2989373	**B2**	**19991213**		
PRAI	**JP 1992-116232**		**19920508**		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 05315628	ICM	**H01L031-04**

AB The process comprises coating a side (S1) of a Si **substrate** with a **SiO2**-based material, **coating** another side (S2) with a dopant-containing material, heating the **substrate** to form a PN **bonding layer** on S2 and to form an **oxide film** on S2 and a Si **oxide film** on S1 simultaneously, and retaining the both films. **Passivation films** are formed on both sides by the easy process.

IT Photoelectric devices, solar
(silicon, **substrates coated** with **oxide films** for)
IT 7631-86-9, Silica, uses
RL: USES (Uses)
(coatings, on silicon **substrates**, for solar cells)
IT 7723-14-0, Phosphorus, uses
RL: USES (Uses)
(dopants, **oxide** coatings containing, on silicon **substrates**, for solar cells)
IT 7440-21-3, Silicon, uses
RL: USES (Uses)
(**substrates**, **oxide film** formation on, for solar cells)

17/TI,PN,PD,AN,AD,IC,AB,AB,K/3 (Item 3 from file: 348)

Conversion of silica precursors to silica at low temperatures.

PATENT (CC, No, Kind, Date): EP 461782 A2 911218 (Basic)
EP 461782 A3 920129
EP 461782 B1 931006
APPLICATION (CC, No, Date): EP 91304882 910530;
PRIORITY (CC, No, Date): US 532828 900604
INTERNATIONAL PATENT CLASS: H01L-021/316; C04B-035/14; C04B-035/64;

ABSTRACT EP 461782 A2

This invention relates to a low temperature method of converting silica precursor coatings to ceramic silica coatings. The method comprises applying a **silica** precursor coating to a **substrate**, exposing the coating to an environment comprising ammonium hydroxide and/or wet ammonia vapors and subjecting the coating to a temperature sufficient to yield the ceramic coating. The methods of the invention are particularly applicable to applying coatings on electronic devices.

...SPECIFICATION infra. Alternatively, the modifying ceramic oxide precursor may be hydrolyzed or partially hydrolyzed, dissolved in the solution comprising the solvent and H-resin and then **immediately** applied to the **substrate**. Various facilitating measures such as stirring or agitation may be used as necessary to produce said solutions.

If compounds of the formula R(sub(x...silicon carbon containing coatings, silicon nitrogen containing coatings,silicon nitrogen carbon containing coatings and/or diamond like carbon coatings.

In a dual layer system, the **second passivation layer** may comprise silicon containing coatings, silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings, an additional silicon dioxide and modifying ceramic oxide coating or a diamond-like carbon coating. In a triple layer system, the **second passivation layer** may comprise silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings, an additional silicon dioxide and modifying ceramic oxide coating or...

17/TI,PN,PD,AN,AD,IC,AB,AB,K/4 (Item 4 from file: 348)

Amine catalysts for the low temperature conversion of silica precursors to silica.
Amin-Katalysatoren fur die Umwandlung von Kieselsaure-Vorprodukten zu Kieselsaure bei niedriger Temperatur.
Catalyseur a base d'amines pour la conversion a temperature basse de produits preliminaires de l'acide silicique en acide silicique.
PATENT (CC, No, Kind, Date): EP 460868 A1 911211 (Basic)
EP 460868 B1 940518
APPLICATION (CC, No, Date): EP 91304881 910530;
PRIORITY (CC, No, Date): US 532705 900604
INTERNATIONAL PATENT CLASS: C04B-035/14; C04B-041/52;

ABSTRACT EP 460868 A1
This invention relates to a low temperature method of converting coatings of hydrogen silsesquioxane resin or hydrolyzed or partially hydrolyzed R(sub(x))Si(OR)(sub(4-x)) to ceramic silica coatings. The method comprises applying a **silica** precursor coating to a **substrate**, exposing the coating to an environment comprising an amine and subjecting the coating to a temperature sufficient to yield the ceramic coating. The methods of the invention are particularly applicable to applying coatings on electronic devices.

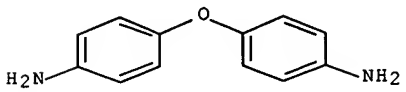
...SPECIFICATION Alternatively, the modifying ceramic oxide precursor may be hydrolyzed or partially hydrolyzed, dissolved in the solution comprising the solvent and the H-resin and then **immediately** applied to the **substrate**. Various facilitating measures such as stirring or agitation may be used as necessary to produce said solutions.
If compounds of the formula R(sub(x...

...sub(4-x)) are to be mixed with modifying ceramic oxide precursors, either or both of these compounds may be hydrolyzed or partially hydrolyzed before **or** after mixing. For **highly** reactive modifying ceramic oxide precursors such as compounds with propoxide, isopropoxide, butoxide, isobutoxide or acetylacetonate substituents, it is preferred that the modifying ceramic oxide precursors...layers, silicon containing coatings, silicon carbon containing coatings, silicon nitrogen containing coatings and/or silicon nitrogen carbon containing coatings.
In a dual layer system, the **second passivation layer** may comprise silicon containing coatings, silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating. In a triple layer system, the **second passivation layer** may comprise silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating and the third barrier coating may comprise silicon coatings, silicon carbon-containing coatings, silicon nitrogen-containing coatings and silicon carbon nitrogen containing coatings.
The silicon-containing coating described above is applied by a method selected from the group consisting of (a) chemical vapor deposition of a silane, halosilane, halodisilane, halopolysilane or mixtures thereof, (b) plasma enhanced chemical...

L151 **ANSWER** 4 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1990:208983 HCAPLUS Full-text
DN 112:208983
ED Entered STN: 26 May 1990
TI **Surface passivation and barrier height enhancement of n-type indium gallium arsenide (In0.53Ga0.47As) Schottky barrier photodiodes**
AU Lee, D. H.; Li, Sheng S.
CS Univ. Florida, Gainesville, FL, 32611, USA
SO Proceedings of SPIE-The International Society for Optical Engineering **(1989)**, 1144(Int. Conf. Indium Phosphide Relat. Mater. Adv. Electron. Opt. Devices, 1st), 174-9
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
CC 76-5 (Electric Phenomena)
Section cross-reference(s): 73
AB Studies of surface passivation and new barrier height enhancement of n-type In0.53Ga0.47As Schottky barrier photodiodes have been carried out. For surface passivation, various dielec. films such as **SiO2, Si3N4 and polyimide** were studied and compared. The results showed that MSM photodiodes passivated with polyimide film yielded the lowest leakage current, whereas the SiO2 passivated device had the highest leakage current. A new barrier height enhancement method on n-type In0.53Ga0.47As Schottky diodes was developed by depositing a thin graded superlattice of In0.53Ga0.47As/In0.52Al0.48As (10 periods, 60 Å/per period) on n-In0.53Ga0.47As epilayer using MBE technique. Effective barrier heights of .apprx. 0.71 and .apprx. 0.60 eV were obtained for Au and Cr Schottky contacts deposited on this graded superlattice, resp.
IT **7631-86-9, Silicon dioxide, uses and miscellaneous**
12033-89-5, Silicon nitride, uses and miscellaneous
25038-81-7, Dupont PI 2555
(**passivation** with, of gallium indium arsenide Schottky barrier **photodiodes**, leakage current in relation to)
IT **25038-81-7**, Dupont PI 2555
(**passivation** with, of gallium indium arsenide Schottky barrier **photodiodes**, leakage current in relation to)
RN 25038-81-7 HCAPLUS
CN 1H,3H-Benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, polymer with 4,4'-oxybis[benzenamine] (9CI) (CA INDEX NAME)

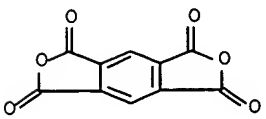
CM 1

CRN 101-80-4
CMF C12 H12 N2 O



CM 2

CRN 89-32-7
CMF C10 H2 O6



L151 **ANSWER** 3 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1991:186959 HCAPLUS Full-text
DN 114:186959
ED Entered STN: 17 May 1991
TI **Photosensitive polyimide compositions**
IN Okunoyama, Teru; Imagawa, Yasuko
PA Toshiba Chemical Corp., Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 02284924**	**A2**	**19901122**	**JP 1989-108065**	**19890427**
PRAI	**JP 1989-108065**		**19890427**		

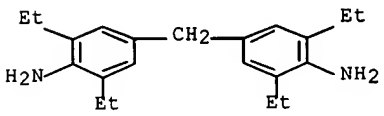
AB The title compns., heat- and chemical-resistant and useful as elec. insulators and passivation films in electronic devices, contain polyimides prepared from 3,3',4,4'-benzophenonetetracarboxylic acid or its dianhydride (I) or alkyl esters and aromatic diamines containing ≥90 mol% mixture of H2NZ1(Et)(R1)ZZ1(R2)(Et)NH2 and CO(Z1NH2)2 (Z = CH2, O, SO2, CMe2, C(CF3)2, S; R1-2 = Me, Et, OMe, OEt; Z1 = C6H4, cyclohexylene; ring substituents are all ortho to NH2). Thus, 232.5 g 4,4'-methylenebis(2,6- diethylaniline), 36.0 g 3,3'-diaminobenzophenone, and 32.2 g I in N-methylpyrrolidone were stirred at 0° for 6 h and then with Ac2O and pyridine at 100° for 3 h to give 59 g polyimide (II). A cyclohexanone solution of II was coated on a Si wafer, dried, cured by UV through a mask, developed, washed, and dried to give an insulating film with 5% weight loss temperature 495°, glass temperature 295°, and no change after 10 min in C2HCl3, acids, or alkalies; vs. 351, 150, and change, resp., for a conventional photosensitive polyamide.

IT **133396-93-7 133396-94-8 133396-95-9**
(**photosensitive**, chemical- and heat-resistant, for elec. insulation and **passivation**)

RN 133396-93-7 HCAPLUS
CN 1,3-Isobenzofurandione, 5,5'-carbonylbis-, polymer with bis(3-aminophenyl)methanone and 4,4'-methylenebis[2,6-diethylbenzenamine]

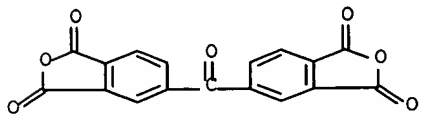
CM 1

CRN 13680-35-8
CMF C21 H30 N2



CM 2

CRN 2421-28-5
CMF C17 H6 O7



CM 3

CRN 611-79-0
CMF C13 H12 N2 O

L151 **ANSWER 2 OF 9 HCAPLUS COPYRIGHT ACS on STN**
AN 1991:248595 HCAPLUS Full-text
DN 114:248595
ED Entered STN: 28 Jun 1991
TI Photopolymerizable resin compositions for passivation films
IN Kihara, Naoko; Oba, Masayuki; Mikogami, Yukihiro
PA Toshiba Corp., Japan

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 02261862	**A2**	**19901024**	**JP 1989-83577**	**19890331**
PRAI JP 1989-83577		**19890331**		

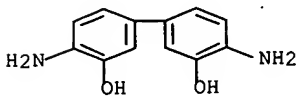
AB Title compns. are prepared polyamide acids prepared from tetracarboxylic dianhydrides and H2NR1NH2 (R1 = divalent organic group containing phenolic OH groups), unsatd. epoxides HCR2:CHR3 (R2 = H, alkyl, aryl; R3 = oxiranyl-terminated organic group), and catalysts. Thus, 21.8 g pyromellitic dianhydride, 21.6 g 4,4'-diaminobiphenyl-3,3'-diol, and N-methylpyrrolidone (I) were stirred at 10° for 5 h and stirred with 12.8 g glycidyl acrylate and 0.7 g Ph3P at 80° for 2 h to give a photocurable composition which was mixed with 3.5 g benzophenone. The mixture was applied on a Si wafer, cured through a neg. photomask in UV light, and soaked in I-MeOH for 5 min to give a good relief pattern.

IT **27082-85-5DP**, reaction products with glycidyl acrylate
31669-98-4DP, reaction products with glycidyl acrylate
122962-65-6DP, reaction products with (glycidoxypropyl)(methacryloyloxypropyl)tetramethyldisiloxane
122988-66-3DP, reaction products with (glycidoxypropyl)(methacryloyloxypropyl)tetramethyldisiloxane
133830-36-1DP, reaction products with (glycidoxypropyl)(methacryloyloxypropyl)tetramethyldisiloxane
133830-86-1DP, reaction products with (glycidoxypropyl)(methacryloyloxypropyl)tetramethyldisiloxane
RL: PREP (Preparation)
(preparation of **photocurable**, for **passivation** film on silicon wafer)

RN 27082-85-5 HCAPLUS
CN 1H,3H-Benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, polymer with 4,4'-diamino[1,1'-biphenyl]-3,3'-diol (9CI) (CA INDEX NAME)

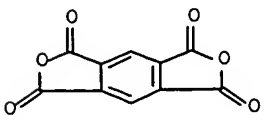
CM 1

CRN 2373-98-0
CMF C12 H12 N2 O2



CM 2

CRN 89-32-7
CMF C10 H2 O6



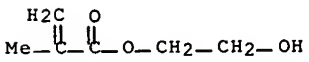
RN 31669-98-4 HCAPLUS

L151 **ANSWER** 5 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1989:214790 HCAPLUS Full-text
DN 110:214790
ED Entered STN: 10 Jun 1989
TI Preparation and properties of soluble and colorless fluorine-containing **polyimide precursors**
AU Omote, Toshihiko; Koseki, Kenichi; Yamaoka, Tsuguo
CS Fac. Eng., Chiba Univ., Chiba, 260, Japan
SO **Journal of Photopolymer Science and Technology (1988), 1(1), 120-1**
CODEN: JSTEEW; ISSN: 0914-9244
DT Journal
LA English
CC 42-10 (Coatings, Inks, and Related Products)
Section cross-reference(s): 38, 76
AB In order to form passivation coatings, alpha particle barriers, inter-layer dielecs., etc., by a photo-lithog. technique, four kinds of photosensitive polyimide precursors were prepared by polycondensation of diamines with tetracarboxylic dianhydride followed by esterification with 2-hydroxyethyl methacrylate. The solubility and transparency at 365 nm wavelength were compared to disclose that the presence of CF3 groups in the amine structure makes the precursor more readily soluble in various organic solvents and optically more transparent. A 3-μm-thick film of the precursor from 2,2-bis(3-amino-4-methylphenyl)hexafluoropropane and biphenyltetracarboxylic dianhydride containing 1 weight% of BP and 5 weight% of MK as photo-initiator provided on a Si wafer gave 0.5 μm L&S patterns with an aspect ratio of 6.0 in spite of neg. working mode.
IT **9043-05-4DP**, esters with hydroxyethyl methacrylate
69280-29-1P 120621-33-2P 120720-51-6P
120720-52-7P 120720-53-8P
(preparation of **photosensitive**, for **passivation** coatings, alpha particle barriers and interlayer dielecs.)
RN 9043-05-4 HCAPLUS
CN Poly[oxy-1,4-phenyleneiminocarbonyl(dicarboxyphenylene)carbonylimino-1,4-phenylene]

RN 69280-29-1 HCAPLUS
CN 1H,3H-Benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, polymer with 4,4'-oxybis[benzenamine], 2-[(2-methyl-1-oxo-2-propenyl)oxy]ethyl ester

CM 1

CRN 868-77-9
CMF C6 H10 O3

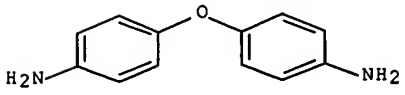


CM 2

CRN 25038-81-7
CMF (C12 H12 N2 O . C10 H2 O6)x
CCI PMS

CM 3

CRN 101-80-4
CMF C12 H12 N2 O



L115 **ANSWER** 3 OF 3 **HCAPLUS COPYRIGHT ACS on STN**
AN 1990:563844 HCAPLUS Full-text
DN 113:163844
ED Entered STN: 27 Oct 1990
TI **Semiconductor** devices coated by **passivation films**
IN Miyamoto, Yasunori
PA Matsushita Electric Works, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM **H01L021-318**
ICS **H01L021-316**
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 02110930	**A2**	**19900424**	**JP 1988-263777**	**19881019**
PRAI JP 1988-263777		**19881019**		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 02110930	ICM	**H01L021-318**
	ICS	**H01L021-316**

AB A **passivation** film coated over a **semiconductor**-mounted **substrate** comprises Si oxide, Si nitride oxide, and Si nitride layers. The internal stresses of above Si oxide, Si nitride oxide, and Si nitride may be 0.8-1 + 109, 1-2 + 109, and 2-4 + 109 dyn/cm2, resp. The 3-layer film prevents formation of cracks during heat-treatment.

IT **Semiconductor** devices
(**passivation films** for, **triple layer** coating for)
IT 7631-86-9, Silicon oxide (SiO2), uses and miscellaneous 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, properties
RL: USES (Uses)
(**passivation** film **laminated** with)

17/TI,PN,PD,AN,AD,IC,AB,AB,K/5 (Item 5 from file: 348)

Coatings for microelectronic devices and substrates
Uberzugsschicht fur mikroelektronische Anordnungen und Substrate
Couche de revetement pour dispositifs et substrats micro-electroniques
PATENT (CC, No, Kind, Date): EP 442632 A2 910821 (Basic)
EP 442632 A3 920401
EP 442632 B1 961127
APPLICATION (CC, No, Date): EP 91300701 910130;
PRIORITY (CC, No, Date): US 480399 900215
INTERNATIONAL PATENT CLASS: H01L-021/314; H01L-021/48; H01L-021/312; C04B-041/87; C04B-041/89;

ABSTRACT EP 442632 A2
The present invention relates to a method of forming a ceramic or ceramic-like coating on a substrate, especially electronic devices, as well as the substrate coated thereby. The method comprises coating said substrate with a solution comprising a solvent, hydrogen silsesquioxane resin and a modifying ceramic oxide precursor selected from the group consisting of tantalum oxide precursors, niobium oxide precursors, vanadium oxide precursors, phosphorous oxide precursors and boron oxide precursors. The solvent is then evaporated to thereby deposit a preceramic coating on the substrate. The preceramic coating is then ceramified by heating to a temperature of between about 40(degree)C. and about 1000(degree)C. This coating, moreover, may be covered by additional passivation and barrier coatings.

...SPECIFICATION present invention also relates to the formation of additional ceramic or ceramic-like coatings on the coating formed above. In a dual layer system, the **second passivation layer** may comprise silicon containing coatings, silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating. In a triple layer system, the **second passivation layer** may comprise silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating...Alternatively, the modifying ceramic oxide precursor may be hydrolyzed or partially hydrolyzed, dissolved in the solution comprising the solvent and the H-resin and then **immediately** applied to the **substrate**. Various facilitating measures such as stirring or agitation may be utilized as necessary to produce said solutions.

The preceramic solution may optionally be catalyzed by...layers, silicon containing coatings, silicon carbon containing coatings, silicon nitrogen containing coatings and/or silicon nitrogen carbon containing coatings.

In a dual layer system, the **second passivation layer** may comprise silicon containing coatings, silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating. In a triple layer system, the **second passivation layer** may comprise silicon carbon-containing coatings, silicon nitrogen-containing coatings, silicon carbon nitrogen containing coatings or an additional silicon dioxide and modifying ceramic oxide coating...

...SPECIFICATION present invention also relates to the formation of additional ceramic or ceramic-like coatings on the coating formed above. In a dual layer system, the **second passivation layer** may comprise silicon-containing coatings, silicon-carbon-containing coatings, silicon-nitrogen-containing coatings, silicon-carbon-nitrogen-containing coatings or an additional silicon dioxide and modifying ceramic oxide coating. In a triple layer system, the **second passivation layer** may comprise

silicon-carbon-containing coatings, silicon-nitrogen-containing coatings, silicon-carbon-nitrogen-containing coatings or an additional silicon dioxide and modifying ceramic oxide coating...Alternatively, the modifying ceramic oxide precursor may be hydrolysed or partially hydrolysed, dissolved in the solution comprising the solvent and the H-resin, and then **immediately** applied to the **substrate**. Various facilitating measures such as stirring or agitation may be utilized as necessary to produce said solutions.

The preceramic solution may optionally be catalysed by...layers, silicon-containing coatings, silicon-carbon-containing coatings, silicon-nitrogen-containing coatings and/or silicon-nitrogen-carbon-containing coatings.

In a dual layer system, the **second passivation layer** may comprise silicon-containing coatings, silicon-carbon-containing coatings, silicon-nitrogen-containing coatings, silicon-carbon-nitrogen-containing coatings or an additional silicon dioxide and modifying ceramic oxide coating. In a triple layer system, the **second passivation layer** may comprise silicon-carbon-containing coatings, silicon-nitrogen-containing coatings, silicon-carbon-nitrogen-containing coatings or an additional silicon dioxide and modifying ceramic oxide coating...

17/TI,PN,PD,AN,AD,IC,AB,AB,K/6 (Item 6 from file: 348)

MOS field-effect transistor and method of making the same.
PATENT (CC, No, Kind, Date): EP 255133 A2 880203 (Basic)
EP 255133 A3 881207
EP 255133 B1 931006
APPLICATION (CC, No, Date): EP 87111043 870730;
PRIORITY (CC, No, Date): JP 86178889 860731
INTERNATIONAL PATENT CLASS: H01L-029/10; H01L-029/784;

ABSTRACT EP 255133 A2
The present invention relates to a semiconductor device comprising a semiconductor substrate (1) of a first conductivity type or an insulator, a source (4) comprising an impurity layer of a second conductivity type disposed on said semiconductor **substrate** or said **insulator**, a drain (5) comprising an impurity layer of the second conductivity type disposed on said semiconductor **substrate** or said **insulator**, an impurity layer (6) of the first conductivity type formed between said source and said drain, a gate (3) formed on said impurity layer of the first conductivity type via an insulation film, and an impurity layer (7) of the second conductivity type having an impurity concentration lower than that of said source and said drain, said impurity layer of the second conductivity type being disposed between said source, said drain and said impurity layer of the first conductivity type, and said semiconductor substrate of the first conductivity type or said insulator.

...SPECIFICATION layer 2 located under the gate 3 by the gate voltage V(sub(GS)). Accordingly, a channel is formed on the surface of the semiconductor **substrate** 1 **immediately under the insulation layer 2**. When the illustrated MOSFET is turned ON, therefore, the drain current is distributed so as to be concentrated to a range of several nm (ten angstroms) in depth from the...thickness of 800 nm (8,000 A) and worked to have a wiring shape by the photolithography technique. The electrode 9 is formed. Lastly the **passivation film** 11 is deposited.
By means of the processing steps heretofore described, the MOSFET according to the present invention explained by referring to Figs. 2 to ...

...CLAIMS a first conductivity type (p) or an insulator;
a source (4) comprising an impurity layer of a second conductivity type (n) disposed on said semiconductor **substrate** or said **insulator**;
a drain (5) comprising an impurity layer of the second conductivity type disposed on said semiconductor **substrate** or said **insulator**;
an impurity layer (6) of the first conductivity type formed between said source and said drain;
a gate (3) formed on said impurity layer of...

...Claim 1, wherein said semiconductor substrate of the first conductivity type has such a structure that a monocrystalline thin semiconductor film is formed on an **insulator substrate**.
3. A fabrication method of semiconductor device comprising the steps of:
(1) forming an oxide film (2) on the surface of a semiconductor substrate (1...

...the surface of an insulator;
(2) forming an impurity layer (7) by implanting impurity ions of a second conductivity type from the top of said **oxide** film into said **substrate** or said **insulator**;
(3) forming a polysilicon gate (3) on said oxide film;
(4) forming a source (4) and a drain (5) by implanting impurity ions of the...

L154 **ANSWER** 8 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1988:503163 HCAPLUS Full-text
DN 109:103163
ED Entered STN: 17 Sep 1988
TI **Passivation of semiconductor devices with polyimides**
IN Eguchi, Masuichi; Hiramoto, Yoshi; Manabe, Shinichi
PA Toray Industries, Inc., Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 63015424**	**A2**	**19880122**	**JP 1986-160172**	**19860708**
	JP 07116407	**B4**	**19951213**		
PRAI	**JP 1986-160172**		**19860708**		

AB A **polyimide**-type varnish, consisting of polyamic acids having a structural repeating unit COR1(CO2H)mCONHR2NH (R1 = tri- or tetravalent organic group; R2 = divalent organic group; m = 1, 2), tertiary amines, and R3nSi(OH)4-n (R3 = monovalent organic group; n = 1, 2, 3) or their partial condensates, is applied on exposed parts of a p-n junction and then heat-treated for passivation of semiconductor devices. Semiconductor devices having high reliability can be prepared Benzophenonetetracarboxylic acid dianhydride-bis(3-aminopropyl)tetramethyldisiloxane-diaminodiphenyl ether-pyromellitic acid dianhydride copolymer was mixed with dimethylaminoethyl methacrylate and OCD Type 2 (silanol compound), applied on a p-n junction of a power diode, and heat-treated to give a passivation coating having excellent resistance to exposure in pressurized saturated vapor at 120°.

IT **116164-52-4**
(passivation coating containing, for semiconductors)
RN 116164-52-4 HCAPLUS
CN 1H,3H-Benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, polymer with 5,5'-carbonylbis[1,3-isobenzofurandione], ar,ar'-oxybis[benzenamine] and 3,3'-(1,1,3,3-tetramethyl-1,3-disiloxanediyl)bis[1-propanamine]

CM 1

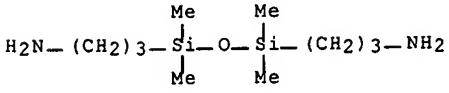
CRN 27133-88-6
CMF C12 H12 N2 O
CCI IDS

D1—NH2

1/2 (D1—O—D1)

CM 2

CRN 2469-55-8
CMF C10 H28 N2 O Si2



CM 3

6/TI,PN,PD,AN,AD,IC,AB,AB,K/2 (Item 2 from file: 348)

A trench-incorporated monolithic semiconductor capacitor and high density dynamic memory cells including the capacitor.

PATENT (CC, No, Kind, Date): EP 220392 A2 870506 (Basic)
EP 220392 A3 890614
EP 220392 B1 930505
APPLICATION (CC, No, Date): EP 86110459 860729;
PRIORITY (CC, No, Date): US 792996 851030
INTERNATIONAL PATENT CLASS: H01L-027/10; H01L-021/82;

ABSTRACT EP 220392 A2

A high density **integrated circuit** structure, for example a dynamic memory cell, is described which includes an active/passive device in combination with a capacitor structure. The capacitor structure is of the polysilicon-oxide-silicon type and is formed on the sidewalls of a mesa-shaped and dielectrically isolated region of silicon material resulting from the formation of an isolation trench in the silicon. The trench is filled with a plastic material, such as polyimide. The capacitor is formed by the isolated region of silicon material (14) which functions as the first capacitor plate, a doped polysilicon layer (22a) provided on the vertical walls of the mesa serving as the second capacitor plate and a thin dielectric layer (21) interposed between the two plates serving as the capacitor's dielectric. Since the polysilicon is wrapped around the periphery of the mesa as a coating on the vertical sidewalls thereof, it gives rise to a large storage capacitance without an increase in the cell size.

...CLAIMS serving as the dielectric for said capacitor structure;
d) forming a thin layer (22) of doped polysilicon on the resulting structure;
e) forming a **dual passivating layer** of silicon dioxide and silicon nitride (23, 24), in order, on the resulting structure;
f) removing by using a photolithographic process the nitride-oxide...

...j) making ohmic contacts (25a, 29a) with both said polysilicon tab and the reach-through region.
2. The method of claim 1 further including the **step** of filling said trenches for device isolation purposes with a material (19a) selected from **a** group consisting of polyimide, polysilicon and silicon dioxide.
3. The method of claim 2 wherein said substrate is of the P- type of conductivity.
4. The method of claim 3 wherein said epitaxial layer...

...capacitor.
7. The capacitor structure of claim 6 wherein said insulating layer is silicon dioxide.
8. The capacitor structure of claim 6 further comprising a **passivation** layer covering said conductive polysilicon.
9. The capacitor structure of claim 8 wherein said **passivation** layer is comprised of a thin silicon dioxide layer formed by thermal reoxidation of the polysilicon layer and a silicon nitride overcoat layer.
10. The...location where a capacitor is to be formed;
b) a pattern of substantially vertical isolation trenches extending from one surface of said structure into said **substrate** through said epitaxial layer, thereby delineating a plurality of mesa shaped isolated regions of semiconductor material;
c) **a** conductive polysilicon layer provided at least partially on the vertical sidewalls of said isolated regions where a capacitor structure is needed thereby forming the first...

...of the second electrode plate of the capacitor.

18. A high density memory according to claim 17 wherein said active device is either a vertical **NPN** bipolar transistor or P-**FET**.

19. A high density memory according to claim 13 wherein said substrate is of the P(sup -) type of conductivity and said epitaxial layer is ...

...density memory according to claim 13 wherein said insulating layer is silicon dioxide.

24. A high density memory according to claim 23 further comprising a **passivation** layer formed on said polysilicon layer.

25. A high density memory according to claim 24 wherein said **passivation** layer is comprised of a thin silicon dioxide layer formed by thermal reoxidation of the polysilicon layer and a silicon nitride overcoat layer.

26. A...

...is material selected from the group consisting of polyimide, polysilicon and silicon dioxide.

28. A high density memory according to claim 13 wherein the configuration **of** the base of said mesa-shaped isolated region is selected from the group of configurations consisting of rectangular, square, circular, serpentine, and comb-like configuration...

...including a conductive polycrystalline silicon layer on the sidewall of said trench and said regions which said polycrystalline silicon layer is separated from a semiconductor **substrate** by the capacitor silicon **dioxide** dielectric layer;

an extended portion of said polycrystalline silicon layer extends to the top surface of said regions to act as on contact to said... layer serving as the dielectric for said capacitor structure;

d) forming a thin layer of doped polysilicon on the resulting structure;

e) forming a dual **passivating** layer of silicon dioxide and silicon nitride, in order, on the resulting structure;

f) removing by using a photolithographic process the nitride-oxide-polysilicon composite...

...CLAIMS structure de condensateur,

d) la formation d'une couche mince (22) de polysilicium dope sur la structure obtenue,

e) la formation d'une couche de **passivation** double de dioxyde de silicium et de nitrure de silicium (23, 24), afin d'effectuer les operations suivantes sur la structure obtenue,

f) le retrait...

L151 **ANSWER** 9 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1983:5047 HCAPLUS Full-text
DN 98:5047
ED Entered STN: 12 May 1984
TI Siloxanes
IN Berger, Abe
PA M and T Chemicals Inc. , USA

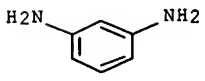
PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 54426	A2	19820623	EP 1981-305864	19811214
EP 54426	A3	19820811		
US 4395527	**A**	**19830726**	**US 1980-216599**	**19801215**

AB Monomers or polymers containing the linkage ZZ1Z2SiR2(OSiR12)x(OSiR2R3)y(OSiR4 R5)xOSiR2Z2Z1Z (Z = substituted or unsubstituted aromatic compound; Z1 = O, S, SO, SO2, SO2NH, NHSO2, CONH, NHCO, CO2, O2C; Z2 = substituted or unsubstituted hydrocarbylene; R, R1, R2, R3, R4, R5 = substituted or unsubstituted hydrocarbyl; x, y, z = 0-100) were prepared and used in modification of polyimides and other polymers. Thus, a mixture consisting of 50% aqueous NaOH 43.28, DMSO 112, PhMe 120, and p-aminophenyl [123-30-8] 59.95 parts was heated under N, azeotropically distilled to removed water, stirred 7-8 h while the temperature increased to 122°, cooled to .apprx.80°, treated with 86.6 parts bis(chlorobutyl)tetramethyldisi loxane [72066-91-2] dropwise to maintain the reaction temperature at .apprx.80°, heated .apprx.16 h at 80°, and distilled at 295-300° at 0.5-2 mm Hg to give bis(p-aminophenoxybutyl)tetramethyl disiloxane (I) [72066-92-3] which was a colorless liquid which eventually solidified to a white solid with melting 48-49°. A mixture consisting of I 54.64, m-phenylenediamine 29.94, and n-methylpyrrolidone 636 g was cooled to 0°, treated portionwise over a 4-h period with 127.05 g benzophenone tetracarboxylic dianhydride, stirred 10 h at room temperature to give a dark amber clear viscous solution of the corresponding poly(half-amide) which was coated on a glass slide to .apprx.0.2 mil thickness, heated 2 h at 120°, heated 2 h at 135°, heated 2 h at 185°, heated 2 h at 250°, and heated 0.5 h at 300° to give a polyimide [**83874-52-6**] coating which bonded tenaciously to the glass slide even after immersion in boiling water for 6 h. The polyimide was excellent as a **passivation and/or protective coating for semiconductor devices** including application of the material to exposed portions of P-N junctions. Low leakage current <0.3 μamps was observed at 0.31 μamps and 2000 V. The polyimide could resist 450° for <1 h.

IT **83874-61-7D**, reaction products with azidodinnamyl chloride
(**photosensitive**)
RN 83874-61-7 HCAPLUS
CN 1,3-Isobenzofurandione, 5,5'-[(1-methylethylidene)bis(4,1-phenyleneoxy)]bis-, polymer with 1,3-benzenediamine and 2,4-diaminophenol

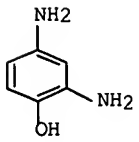
CM 2

CRN 108-45-2
CMF C6 H8 N2



CM 3

CRN 95-86-3
CMF C6 H8 N2 O



L151 **ANSWER** 6 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1985:185995 HCAPLUS Full-text
DN 102:185995
ED Entered STN: 02 Jun 1985
TI Organic solvent-soluble **photosensitive polyimides**
PA Ube Industries, Ltd., Japan; Nippon Telegraph and Telephone Public Corp.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM C08G073-12
CC 37-3 (Plastics Manufacture and Processing)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 59232122	**A2**	**19841226**	**JP 1983-106561**	**19830614**
PRAI JP 1983-106561		**19830614**		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 59232122	ICM	C08G073-12

AB Polyimides useful as elec. insulating materials and **passivation** membranes are copolycondensates of a biphenyltetracarboxylic acid or its dianhydride and aromatic diamines H2NC6H4CH:CHCOR (R = C6H4NH2, CH:CHC6H4NH2) and (H2NC6H4)2Z (Z = O, CO, p-OC6H4SO2C6H4O-p). Thus, 2,3,3',4'-biphenyltetracarboxylic dianhydride 1580, 3,3'- diaminodibenzalacetone 710, and 4,4'-diaminodiphenyl ether 538 mg were mixed in N-methyl-2-pyrrolidone (I) to give a polyamic acid which was dissolved in I and imidated using Ac2O and pyridine to give a polyimide [**96250-25-8**] having inherent viscosity (30°) 0.45, good film formability, solubility in I 10.0%, and heat decomposition temperature 500°. The polyimide film (1.0 μ) was cured by **light** irradiation of 1.3 J/cm2.

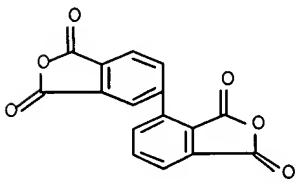
IT **96250-23-6P 96250-24-7P 96250-25-8P**
(preparation and **photochem**. crosslinking of)

IT **96250-23-6P 96250-24-7P 96250-25-8P**
(preparation and **photochem**. crosslinking of)

RN 96250-23-6 HCAPLUS
CN [4,5'-Biisobenzofuran]-1,1',3,3'-tetrone, polymer with 1-(4-aminophenyl)-3-(3-aminophenyl)-2-propen-1-one and 4,4'-oxybis[benzenamine] (9CI) (CA INDEX NAME)

CM 1

CRN 36978-41-3
CMF C16 H6 O6



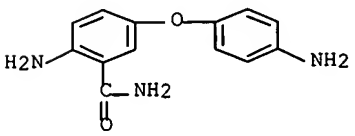
CM 2

CRN 30278-77-4
CMF C15 H14 N2 O

L151 **ANSWER** 8 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1983:90599 HCAPLUS Full-text
DN 98:90599
ED Entered STN: 12 May 1984
TI Characterization of a polyimide passivation on thin film resistor networks
AU Scheiman, Gerald R.
CS Natl. Semiconduct., Santa Clara, CA, USA
SO International Journal for Hybrid Microelectronics (1982), 5(2), 202-4
CODEN: IMICDJ; ISSN: 0277-8270
DT Journal
LA English
CC 38-2 (Plastics Fabrication and Uses)
Section cross-reference(s): 76
AB Under certain conditions, Hitachi PIQ [**55478-71-2**] is an excellent **passivation** material for thin film resistor networks. Adhesion, chemical stability, and wire bond shorting protection are comparable or superior to those of SiO2. PIQ's lithog. and etch properties are within the tolerance required for most thin film circuits. The only drawback to its use is in laser trimmings. PIQ absorbs significant amts. of energy from the 106.4 nm **light** used in most laser trim systems, which precludes its use for most laser-trimmed resistors.
IT **55478-71-2**
(**passivation** by, on elec. resistors)
RN 55478-71-2 HCAPLUS
CN Benzamide, 2-amino-5-(4-aminophenoxy)-, polymer with 1H,3H-benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, 5,5'-carbonylbis[1,3-isobenzofurandione] and 4,4'-oxybis[benzenamine] (9CI) (CA INDEX NAME)

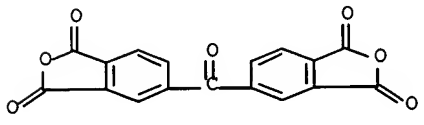
CM 1

CRN 40763-98-2
CMF C13 H13 N3 O2



CM 2

CRN 2421-28-5
CMF C17 H6 O7



CM 3

CRN 101-80-4
CMF C12 H12 N2 O

L151 **ANSWER** 7 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1983:523743 HCAPLUS Full-text
DN 99:123743
ED Entered STN: 12 May 1984
TI **Selective etching of polyimide type resin film**
IN Saiki, Atsushi; Iwayanagi, Takao; Nonogaki, Saburo; Nishida, Takashi; Harada, Seiki
PA Hitachi, Ltd. , Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 82417	A2	19830629	EP 1982-111392	19821209
	EP 82417	A3	19860326		
	EP 82417	B1	19890315		
	JP 58108229	A2	19830628	JP 1981-205326	19811221
	JP 02019972	B4	19900507		
	US 4436583	**A**	**19840313**	**US 1982-445576**	**19821130**
PRAI	JP 1981-205326		19811221		

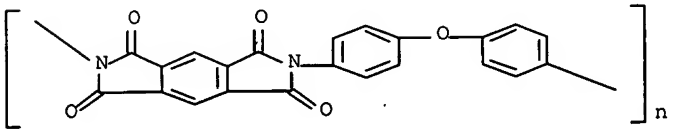
CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
EP 82417	IC	H01L021-312

AB A selective etching method for polyimide resin films useful as interlevel insulation for multilevel metalization or as **passivation** films of transistors, integrated circuits, and large-scale integrated circuits comprises using an etching mask consisting of a neg.-type **photoresist** material prepared by adding a **photosensitive** reagent to an unsatd. ketone polymer as the base resin and an etching solution containing 20-40% hydrazine hydrate and 60-80% of a polyamine. Thus, 2,6-bis(4-azidobenzylidene)-4-methylcyclohexanone [5284-79-7] **photosensitive** reagent was added to poly(isopropenyl Me ketone) [25988-32-3] to give a neg.-type **photoresist** which was dissolved in cyclohexanone, coated on a 2-μ thick PIQ [**55478-71-2**] film, and prebaked 20 min at 85°. A **photomask** having aperture pattern ≥2 μ square was placed in intimate contact with the film and irradiated with UV **light**. The film was **developed** with cyclohexanone, rinsed with Bu acetate, and baked 20 min at 140°. The **developed** film was etched 20 min at 30° with a 3:7 mixture of hydrazine hydrate and ethylenediamine [107-15-3].

IT **25036-53-7 55478-71-2**
(films, etching of, selective, with **photoresists**)

RN 25036-53-7 HCAPLUS
CN Poly[(5,7-dihydro-1,3,5,7-tetraoxobenzo[1,2-c:4,5-c']dipyrrole-2,6(1H,3H)-diyl)-1,4-phenyleneoxy-1,4-phenylene] (9CI) (CA INDEX NAME)



RN 55478-71-2 HCAPLUS
CN Benzamide, 2-amino-5-(4-aminophenoxy)-, polymer with 1H,3H-benzo[1,2-c:4,5-c']difuran-1,3,5,7-tetrone, 5,5'-carbonylbis[1,3-isobenzofurandione] and 4,4'-oxybis[benzenamine] (9CI) (CA INDEX NAME)

CM 1

CRN 40763-98-2
CMF C13 H13 N3 O2

L154 **ANSWER** 9 OF 9 **HCAPLUS COPYRIGHT ACS on STN**
AN 1983:171768 HCAPLUS Full-text
DN 98:171768
ED Entered STN: 12 May 1984
TI Magnetic-bubble memory device
PA Nippon Electric Co., Ltd., Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**JP 57167191**	**A2**	**19821014**	**JP 1981-50092**	**19810403**
PRAI	**JP 1981-50092**		**19810403**		

AB The fabrication of a magnetic-bubble memory device includes the following steps: (1) formation of a conductor film via a 1st spacer (e.g., Al2O3) on a magnetic medium; (2) selective removal of the conductor film to form regions for a pattern of soft magnetic film for detection; (3) successive deposition of a soft magnetic film (e.g., Permalloy) and an insulator film (e.g., SiO2) without removing the mask used in selective removal of the conductor film; (4) selective removal of the soft magnetic and insulator films by left off; (5) formation of the detection and conductor pattern by etching; (6) formation of a 2nd organic-insulator spacer (e.g., **polyimide**) over the extreme surfaces; (7) and formation of a soft-magnetic-film pattern for transferring. A device with planar surfaces and a **2-layer passivation insulator film** is obtained.

IT **Polyimides**, uses and miscellaneous
(spacers, for bubble-domain memory devices)

L148 **ANSWER** 4 OF 4 **HCAPLUS COPYRIGHT ACS on STN**
AN 1972:494621 HCAPLUS Full-text
DN 77:94621
ED Entered STN: 12 May 1984
TI Semiconductor device having a **passivation** film and **insulating** films on a semiconductor **substrate**
PA Hitachi, Ltd.
IC **H01L**

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	**GB 1283769**	**A**	**19720802**	**GB 1969-49538**	**19691008**
PRAI	**JP 1968-73134**	**A**	**19681009**		

AB The amount of **surface** charge induced on a substrate **surface** by an elec. **passivation** film is controlled to a desired value by the insulating films produced on the **passivation** film. E.g., a SiO2 film is formed on a p-type Si **substrate** and a **SiO2**/P2O5 film formed over the SiO2 film. A SiO2/B2O3 film is then deposited over the SiO2/P2O5 film. Electrodes are provided on the **insulating** film and on the **substrate** to form a metal- **oxide**-semiconductor element. The **surface** charge d. on the **substrate** just under the **SiO2** film is 5 + 1011/cm2. When a SiO2/P2O5 film is deposited on the SiO2/B2O3 film, the amount of **surface** charge induced on the Si **surface** is 2 + 1011/cm2. A quadruple or quintuple layer has an even lower **surface** charge d. than the **triple layer**.

IT Semiconductor devices
(coating of, with multilayer insulating films)
IT Electric insulators and Dielectrics
(multilayer coatings, on semiconductor devices)
IT Coating materials
(multilayer, on semiconductor devices)

26/9/9
DIALOG(R)File 2:INSPEC

00119652 INSPEC Abstract Number: A70023377, B70014091
Title: Oxidized SiH/sub 4/ as a diffusion source
Author(s): Mecs, B.M.
Author Affiliation: Stevens Inst. Technol., Hoboken, NJ, USA
Conference Title: 133rd meeting of the Electrochemical Society, Abstracts p.15
Publisher: Electrochem. Soc, New York, NY, USA
Publication Date: 1968 Country of Publication: USA 158 pp.
Conference Sponsor: Electrochem. Soc
Conference Date: 5-9 May 1968 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Abstract: Abstract only given. The mixture of silane (SiH/sub 4/) and phosphine (PH/sub 3/) in the presence of oxygen decomposes, and forms at or above 200 degrees C a continuous **adherent** layer of doped silicon dioxide on a silicon **substrate**. This **oxide** serves as a diffusion source. The apparatus required for deposition is simple. The effects of the deposition variables on the diffusion parameters can be independently determined. The results show that the useful range of **surface** concentration attainable extends from 5*10/sup 15/ cm/sup -3/ to the solid solubility limit. The deposited film is also attractive as a **passivation** and/or insulation layer. Further by substituting diborane (B/sub 2/H/sub 6/) for phosphine a diffusion source for boron is obtainable.